IN THE SPECIFICATION

Please replace the paragraph beginning on page 6, line 14 and ending on page 6, line 21 with the following:

Figure 3 is a diagram illustrating a preferred embodiment of a multiple processor computer system 60 that includes a software-based DMA engine in accordance with the invention. The system may also include a cross bar multipath memory controller 62 (corresponding generally to busses 14 and 33 in Figure 2) and a cross bar multipath peripheral controller 64 which are described in more detail in ~~copending patent application serial number 09/XXX,XXX filed on XXXXXXXXX~~ copending U.S. patent application serial number 09/847,991 filed on May 02, 2001 and entitled "Cross Bar Multipath Resource Controller System and Method" which is owned by the same assignee as the present invention and which is incorporated herein by reference.

Please replace the paragraph beginning on page 7, line 3 and ending on page 7, line 14 with the following:

As shown, the host processor, the coprocessor and the hardware accelerator engine are all connected to the multipath memory controller and the multipath peripheral controller 64 as shown. To control access to the shared resources connected to the multipath memory controller and the multipath peripheral controller, the system 60 may include a semaphore unit 72 which permits the two processors 66, 68 to communicate with each other and control the access to the shared resources. The details of the semaphore unit is described in more detail in copending US patent application ~~number XX/XXX,XXX filed on XXXX,XX 2001 titled "XXX"~~ serial number 09/847,976 filed on May 02, 2001 titled "Multiprocessor Communication System and Method", owned by the same assignee as the present invention and incorporated herein by reference. The semaphore unit permits the processors to negotiate for the access to the shared resources as described above, but then, due to the multipath controllers 62, 64, permits the processors to access the resources over its own bus that is part of the controllers. To control the timing of the controllers 62, 64, a timer/clock 74 is connected to each controller 62, 64.

IN THE TITLE

Please replace the Title of the Invention with the following:

"Software Direct Memory Access Engine for Multiple Processor Systems"